WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell storing data;

a pair of bit lines connected to said memory cell;

a sense amplifier provided corresponding to said pair of bit lines and activated in response to a sense amplifier activation signal;

a pair of I/O lines transmitting said data input/output to/from said memory cell via said pair of bit lines; and

a connection gate circuit provided between said pair of bit lines and said pair of I/O lines and electrically connecting said pair of bit lines to said pair of I/O lines when said sense amplifier activation signal and a column selection signal selecting said pair of bit lines are both activated.

2. The semiconductor memory device according to claim 1, wherein

said connection gate circuit includes first and second gates connected in series between said pair of bit lines and said pair of I/O lines,

said first gate conducts in response to said sense amplifier activation signal, and

said second gate conducts in response to said column selection signal.

3. The semiconductor memory device according to claim 2, wherein said connection gate circuit further includes an equalize circuit equalizing potentials of a pair of nodes connecting said first gate with said second gate.

4. The semiconductor memory device according to claim 2, further comprising:

another memory cell storing data;

another pair of bit lines connected to said another memory cell;

another sense amplifier provided corresponding to said another pair of bit lines and activated in response to said sense amplifier activation signal; and

another connection gate circuit provided between said another pair of bit lines and said pair of I/O lines and electrically connecting said another pair of bit lines to said pair of I/O lines when said sense amplifier activation signal and another column selection signal selecting said another pair of bit lines are both activated; wherein

said another connection gate circuit includes a third gate conducting in response to said another column selection signal,

said second gate is connected between said pair of bit lines and said first gate, and

said third gate is connected between said another pair of bit lines and said first gate.

5. The semiconductor memory device according to claim 4, further comprising:

at least one first N type transistor turned on in response to said sense amplifier activation signal and activating said sense amplifier and said another sense amplifier; wherein

said first gate is a second N type transistor, and

said second N type transistor is formed in a free space of a region where said at least one first N type transistor is formed.

6. The semiconductor memory device according to claim 1, further comprising:

a logic gate circuit activating its output signal when said sense amplifier activation signal and said column selection signal are activated; wherein

said connection gate circuit includes a gate conducting in response to said output signal from said logic gate circuit.

7. The semiconductor memory device according to claim 6, wherein said logic gate circuit is provided at a shunt portion on a memory cell array where said memory cell is formed.

8. The semiconductor memory device according to claim 6, wherein said logic gate circuit is provided at an array control portion controlling an operation of a memory cell array where said memory cell is formed.

9. The semiconductor memory device according to claim 6, wherein

said connection gate circuit further includes another gate conducting in response to a write mask signal, and

said gate and said another gate are connected in series between said pair of bit lines and said pair of I/O lines.

10. The semiconductor memory device according to claim 9, wherein said connection gate circuit further includes an equalize circuit equalizing potentials of a pair of nodes connecting said gate with said another gate.